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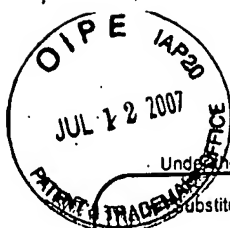
APPLICANT(S): Kenneth M. Williams
APPLICATION NO.: 10/630,542
FILED: July 29, 2003
TITLE: Defining Instruction Extensions in a Standard Programming Language
EXAMINER: Isaac Teku Tecklu
GROUP ART UNIT: 2191
ATTY.DKT.NO.: PA2221US

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**List of Co-Pending Patents or Patent Applications That May Be Directed
Towards Similar Subject Matter**

Examiner's Initials	Application Number	Docket Number	First-Named Inventor	Title	Filing Date
	10/404,706	PA2561US	Scott D. Johnson	Extension Adapter	03-31-2003
	10/686,882	PA2594US	Kenneth Williams	Instruction Set for Efficient Bit Stream and Byte Stream I/O	10-15-2003
	10/750,714	PA2683US	Ricardo Gonzalez	Systems and Methods for Software Extensible Multi-Processing	12-31-2003
	10/815,453	PA2718US	Ricardo Gonzalez	Configuring a Multi-Processor System	03-31-2004
	11/021,247	PA2838US	Ricardo Gonzalez	Systems and Methods for Selecting Input/Output Configuration in an Integrated Circuit	12-21-2004
	11/129,146	PA3036US	Ricardo Gonzalez	Long Instruction Word Processing with Instruction Extensions	05-12-2005
	11/099,280	PA3049US	Jeffrey M. Arnold	Video Processing System with Reconfigurable Instructions	04-04-2005
	11/204,555	PA3350US	Jeffrey M. Arnold	Programmable Logic Configuration for Instruction Extensions	08-15-2005
Examiner's Signature:	//Isaac Tecklu/				Date 03/04/2008

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PTO/SB/08A (09-08)

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Attorney Docket Number	PA2221US

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US- 6,237,079 B1	05-22-2001	Stoney	
		US- 5,488,612	01-30-1996	Heybruck	
		US- 5,847,578	12-08-1998	Noakes et al.	
		US- 6,415,424 B1	07-02-2002	Arimilli et al.	
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		US- 5,652,875	07-29-1997	Taylor	
		US- 5,696,956	12-09-1997	Razdan et al.	
		US- 5,784,636	07-21-1998	Rupp	
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		US- 6,732,354 B2	05-04-2004	Ebeling et al.	
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		US- 2003/0108119 A1	06-12-2003	Mohebbi et al.	
		US- 6,721,884 B1	04-13-2004	De Oliveira Kastrup Pereira et al.	
		US- 6,426,648 B1	07-30-2002	Rupp	
		US- 7,062,520 B2	06-13-2006	Rupp	
		US- 6,857,110 B1	02-15-2005	Rupp et al.	
		US- 6,744,274 B1	06-01-2004	Arnold et al.	

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		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				
		EP 1 443 417	08-04-2004	STMicroelectronics		
		TW 480818	03-21-2002	Adaptive Silicon, Inc.		
		TW 509798	11-11-2002	Adaptive Silicon, Inc.		
		TW 478252	03-01-2002	Adaptive Silicon, Inc.		

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		US- 6,292,388 B1	09-18-2001	Camarota	
		US- 6,418,045 B2	07-09-2002	Camarota	
		US- 7,000,211 B2	02-14-2006	Arnold	
		US- 6,954,845	10-11-2005	Arnold et al.	
		US- 2003/0196058 A1	10-16-2003	Ramagopal et al.	
		US- 5,636,224	06-03-1997	Voith et al.	
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		BORKAR et al., "iWarp: An Integrated Solution to High-Speed Parallel Computing," 1988, IEEE CH2617-9/88/0000/03300.	
		BARAT, FRANCISCO and RUDY LAUWEREINS, "Reconfigurable Instruction Set Processors: A Survey," 2000, IEEE 0-7695-0668-2/00.	
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		TANENBAUM, ANDREW S., "Modern Operating Systems," 2001, 2nd edition, Prentice Hall, New Jersey, p. 31.	
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		SCOTT, STEVEN L. and GREGORY M. THORSON, "The Cray T3E Network: Adaptive Routing in a High Performance 3D Torus," August 15-16, 1996, HOT Interconnects IV, Stanford University.	
		GOLESTANI, S. JAMALODDIN, "A Sto-and-Go Queuing Framework for Congestion Management," 1990, Proc. of the ACM Symposium on Communications Architectures & Protocols, ACM Press, New York, NY, pp. 8-18.	
		DALLY, WILLIAM J. and CHARLES L. SEITZ, "Deadlock Free Message Routing in Multiprocessor Interconnection Networks," May 10, 1985, Computer Science Department, California Institute of Technology.	

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		GARLAN, DAVID and MARY SHAW, "An Introduction to Software Architecture," January 1994, CMU-CS-94-166, School of Computer Science, Carnegie Mellon University, Pittsburgh, PA.	
		INTEL and HEWLETT-PACKARD, "IA-64 Application Instruction Set Architecture Guide," Revision 1.0, 1999, pp. C-1 through C.	
		HWANG, KAI, "Advanced Computer Architecture: Parallelism, Scalability, Programmability," 1993, McGraw Hill, pp. 182-183.	
		YE, Z.A. et al., "CHIMAERA: a high-performance architecture with a tightly-coupled reconfigurable functional unit," June 10-14, 2000, Proc. of the 27th International Symposium on Computer Architecture, pp. 225-235.	
		MIPS Technologies Inc., "MIPS Extension for Digital Media with 3D," 1996, pp. 1-26.	
		BORGATTI, MICHELE et al., "A Reconfigurable System featuring Dynamically Extensible Embedded Microprocessor, FPGA and Customisable I/O," 2002, IEEE Custom Integrated Circuits Conference, pp. 1-4	
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		US- 6,418,045 B2	07-09-2002	Camarota	
		US- 7,000,211 B2	02-14-2006	Arnold	
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		US- 2003/0196058 A1	10-16-2003	Ramagopal et al.	
		US- 5,636,224	06-03-1997	Voith et al.	
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		INTEL and HEWLETT-PACKARD, "IA-64 Application Instruction Set Architecture Guide," Revision 1.0, 1999, pp. C-1 through C.	
		HWANG, KAI, "Advanced Computer Architecture: Parallelism, Scalability, Programmability," 1993, McGraw Hill, pp. 182-183.	
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PTO/SB/08A (08-03)

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~~CONFIDENTIAL~~ Supplemental Form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	2
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Complete if Known

Application Number	10/630,542
Filing Date	July 29, 2003
First Named Inventor	Kenneth M. Williams
Art Unit	2192
Examiner Name	Isaac Tuku Tecklu
Attorney Docket Number	PA2221US

U. S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

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Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ²
		Country Code ³ *Number ⁴ *Kind Code ⁵ (if known)				
		TW 478252	03-01-2002	Adaptive Silicon, Inc.		
		TW 480818	03-21-2002	Adaptive Silicon, Inc.		
		TW 509798	11-11-2002	Adaptive Silicon, Inc.		

Examiner Signature	/Isaac Tecklu/	Date Considered	03/04/2008
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Attorney Docket Number	PA2221US

Sheet 2 of 2

NON PATENT LITERATURE DOCUMENTS

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		PEDRO DINIZ, et al. "Automatic Synthesis of Data Storage and Control Structures for FPGA-based Computing Engines," 2000 IEEE, pages 91-100.	
		MICHAEL BEDFORD TAYLOR et al., "The Raw Microprocessor: A Computational Fabric for Software Circuits and General-Purpose Programs," March-April 2002, IEEE Micro, pages 25-35	
		ELLIOT WAINGOLD et al., "Baring It All to Software: Raw Machines," Computer, September 1997, 1997 IEEE, pages 86-93.	

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Sheet 2 of 2

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**INFORMATION DISCLOSURE
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Sheet 1 of 2

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Application Number	10/630,542
Filing Date	July 29, 2003
First Named Inventor	Kenneth M. Williams
Art Unit	2192
Examiner Name	Isaac Tuku Tecklu
Attorney Docket Number	PA2221US

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		Number-Kind Code ² (if known)			
		US- 5,850,564	12-15-1998	Ting et al.	
		US- 6,167,502	12-26-2000	Pechanek et al.	
		US- 5,684,980	11-04-1997	Casselman	
		US- 6,996,709	02-07-2006	Arnold et al.	
		US- 6,883,084	04-19-2005	Donohoe	
		US- 6,557,092	04-29-2003	Callen	
		US- 6,831,690	12-14-2004	John et al.	
		US- 6,343,337	01-29-2002	Dubey et al.	
		US- 5,299,317	03-29-1994	Chen et al.	
		US- 5,293,489	03-08-1994	Furui et al.	
		US- 5,274,782	12-28-1993	Chalasani et al.	
		US- 5,247,689	09-21-1993	Ewert	
		US- 5,055,997	10-08-1991	Sluiter et al.	
		US- 5,471,628	11-28-1995	Phillips et al.	
		US- 2003/0046513	03-06-2003	Furuta et al.	
		US- 2004/0186872	09-23-2004	Rupp	
		US- 10/746,018	12-23-2003	Rupp et al.	
		US-			
		US-			

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Date
Considered

03/04/2008

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**INFORMATION DISCLOSURE
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Application Number	10/630,542
Filing Date	July 29, 2003
First Named Inventor	Kenneth M. Williams
Art Unit	2192
Examiner Name	Isaac Tuku Tecklu
Attorney Docket Number	PA2221US

Sheet 2 of 2

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		KAI HWANG, "Advanced Computer Architecture: Parallelism, Scalability, Programmability," 1st Edition, Chapter 2, pp. 75-97, copyright 1993, McGraw-Hill, Inc., USA.	

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Sheet 1

of 2

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Sheet	2	of	2		

[illegible]

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